Changes Approved 10/20/04 JRL

IN THE SPECIFICATION:

Please delete the paragraph beginning on page 7, line 1, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

One particular embodiment of the LBIST domain 160 is conceptually illustrated in FIG. 2. In this-particular embodiment, the LBIST engine 110 comprises an LBIST state machine 210 and a pattern generator 230. The LBIST domain 160 also includes a multiple input signature register ("MISR") 220. The content of the MISR 220 is the LBIST signature 130 in **FIG. 1.** The pattern generator 230 is, more precisely, a pseudo random pattern generator ("PRPG"). In the illustrated embodiment, the LBIST engine 110 is externally configured by a CONFIGURATION signal with a vector count and a PRPG seed for the pattern generator 230. The LBIST engine 110 is configured by a ~~66-bit~~ 65-bit signal received through the testing interface 180 in which 32 bits contain the vector count and 33 bits contain the PRPG seed. Thus, the pattern generator 230 is programmable, as is the LBIST engine 110 as a whole. However, the invention is not so limited and other techniques may be employed for configuring the LBIST engine 110. For instance, these values may be hardcoded or hardwired in alternative embodiments.

Please delete the paragraph beginning on page 9, line 17, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

In accordance with yet another aspect of the invention, the content of the LFSR with which the pattern generator 230 is implemented and the register with which the MISR 220 is implemented are generated using different primitive polynomials to prevent failures disguised by aliasing. The content of the LFSR in the illustrated embodiment is based on the 31-bit primitive polynomial $x^{31} + x^3 + 1$ and the content of the MISR 220 is based on the 32-bit primitive polynomial $x^{32} + x^{18} + x + 1$. If the pattern generator 230 enters an all zero state, the error indicator will be activated and stored in bit *B33* of the MISR 220. In this particular embodiment, the even outputs of the LFSR (bits ~~*B26*~~ *B30* to

Bo) supply the scan pattern to the inputs of the scan chains 1 to 23, respectively. The MISR 220 has inputs that EXCLUSIVEOR into the odd register bits *B7* through *B31* and bit *B0* during the scan operation. Alternative embodiments may omit this aspect of the invention, however.

Please delete the paragraph beginning on page 9, line 29, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

The LBIST engine 110 provides two level sensitive scan device ("LSSD") clock signals, shown in **FIG. 9,** to the level sensitive scan devices (not shown) in the core 900. Both of these clock signals are normally low, but alternately pulse high when the LBIST state machine 210 is in the scan state 330. After the scan chains are flushed, the MISR 220 (shown in FIG. 2) collects the scan data. The LBIST engine 110 also outputs two step clock signals LBIST STEP CLKC and LBST STEP ~~STEPE~~ CLKE. The step clock signal LBIST STEP CLKC actually comprises three signals LBIST_STEP CLKC1, LBIST STEP CLKC2, and LBIST STEP CLKC3. The LBST_STEP CLKE clock signal, normally high, enables the LBST STEP CLKC1 through to the core latches (not shown) *via* the core logic clock signal splitters (not shown) of the core 900. The LBST STEP CLKC2 is enabled by the LBST STEP CLKE clock signal through the clock signal splitters (not shown) of the low power register array ("LPRA") wrappers 905. The LBST STEP CLKE clock signal also enables the LBST STEP CLKC3 through the clock signal splitter (not shown) of the wrappers for the memory components ~~150~~ 190, i. *e.,* the SRAM wrappers 910.

Please delete the paragraph beginning on page 13, line 28, and replace with the following new paragraph. Changes from the original paragraph are highlighted.

In operation, the ASIC ~~100~~ 150 shown in **FIG. 1** may be placed on a vendor-supplied tester 915, shown in **FIG. 9,** typically with several other ASICs ~~100~~ 150 (not shown). Alternatively, the ASIC ~~100~~ 150 may be tested in a live system including a live

system controller ~~925~~ 915 including a JTAG controller ~~915~~ 920. The MBIST engine 120 includes a MBIST state machine 610, shown in **FIG. 6,** designed for use with this particular vendor-supplied tester 915. In the illustrated embodiment, the JTAG controller 920 employs JTAG protocols and testing hardware, and so the testing interface 180 is a JTTAP controller. As was noted above, the LBIST and MBIST capabilities of the dual mode BIST controller 100 may be utilized separately or conjunctively. Furthermore, the LBIST and the MBIST may be performed in parallel or in serial. However, the following discussion will contemplate a conjunctive use in serial. It is nevertheless to be understood that only one or the other may be employed in alternative embodiments.